REMARKS

Claims 1, 3-8, 10-15 and 17-21 are pending in the present application. Claims 1, 8 and 15 have been amended. Claims 2, 9 and 16 have been canceled.

Priority Under 35 U.S.C. 119

Applicant notes the Examiner's acknowledgement of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the priority document.

Claim Rejections – 35 U.S.C. 103

Claims 1-21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Leung et al. reference (U.S. Patent No. 6,400,300), in view of the Segawa et al. reference (U.S. Patent No. 5,523,721). This rejection is respectfully traversed for the following reasons.

The digital-to-analog converting circuit of claim 1 includes in combination a first potential terminal for supplying a first potential; a second potential terminal for supplying a second terminal; an output node; a first resistor circuit; a first switching circuit "having a plurality of first switches each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node"; a second resistor circuit; a second switching circuit "having a plurality of second switches each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node"; and a control circuit.

Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

The Examiner has alleged that Fig. 1 of the Leung et al. reference discloses all the features of claim 1, except for a second switching circuit "having a plurality of second switches each of which is connected between the second potential terminal and one of the second connecting points and the second node". In order to overcome this acknowledged deficiency of the Leung et al. reference, the Examiner has relied upon Fig. 6 of the Segawa et al. reference. The Examiner has alleged that it would have been obvious to modify the circuit of the Leung et al. reference in view of the Segawa et al. reference "in order to provide a digitally controlled variable gain circuit for outputting an analog output voltage". Applicant respectfully disagrees for the following reasons.

The Examiner has interpreted the resistors below V_{REF} in Fig. 1 of the Leung et al. reference as the first resistor circuit of claim 1, and switches 80 as connected to the corresponding resistors as the plurality of first switches of claim 1. However, each of switches 80 in Fig. 1 of the Leung et al. reference are not connected directly to the V_{REF} terminal, in addition to being coupled to respective ones of first connecting points between the resistors and a first node, as would be necessary to meet the features of claim 1. Similarly, switches 22 in Fig. 1 of the Leung et al. reference are not each connected directly to the ground potential terminal, in addition to being coupled to respective ones of second connecting points between the corresponding resistors and a second node, as would be necessary to meet the further features of claim 1. The

Leung et al. reference as relied upon by the Examiner thus fails to meet the features of the first and second switching circuits of claim 1.

Applicant also respectfully submits that the Segawa et al. reference as secondarily relied upon by the Examiner fails to overcome the above noted deficiencies of the Leung et al. reference. Particularly, switches S_{71} through to S_{78} of switch 70 in Fig. 6 of the Segawa et al. reference are not each connected directly to the ground potential terminal, as would be necessary to meet the features of claim 1. Thus, even if proper motivation existed for combining the prior art as asserted by the Examiner (which motivation Applicant does not admit exists), the prior art as relied on would fail to meet the features of claim 1. Accordingly, Applicant respectfully submits that the digital-to-analog converting circuit of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 1 and 3-7 is improper for at least these reasons.

With further regard to this rejection, the prior art as relied upon by the Examiner does not disclose or even remotely suggest a first switching circuit having a plurality of first switches that are each P-channel type MOS transistors, and a second switching circuit having a plurality of second switches that are each N-channel type MOS transistors. The prior art as relied upon by the Examiner does not disclose MOS switches. The prior art would thus provide no motivation as to why all of first switches should be P-channel type MOS transistors and all of second switches should be N-channel type MOS transistors. Applicant therefore respectfully submits that the digital-

to-analog converting circuit of claim 4 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claim 4 is improper for at least these additional reasons.

The digital-to-analog converting circuit of claim 8 includes in combination a plurality of first switches "each of which is connected directly to the first potential terminal, and to respective ones of the first connecting points and the first node"; and a plurality of second switches "each of which is connected directly to the second potential terminal, and to respective ones of the second connecting points and the second node".

Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose first switches each of which is connected directly to a first potential terminal, and second switches each of which is connected directly to a second potential terminal, as featured in claim 8. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 8 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 8 and 10-14 is improper for at least these reasons. Applicant also respectfully submits that claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 4.

The digital-to-analog converting circuit of claim 15 includes in combination a plurality of first switches "each of which is connected directly to the first potential terminal, and to respective ones of the first connecting nodes and the first node"; and a

plurality of second switches "each of which is connected directly to the second potential terminal, and to respective ones of the second connecting nodes and the second node".

Applicant respectfully submits that the prior art as relied upon by the Examiner does not disclose first switches each of which is connected directly to a first potential terminal, and second switches each of which is connected directly to a second potential terminal, as would be necessary to meet the features of claim 15. Applicant therefore respectfully submits that the digital-to-analog converting circuit of claim 15 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 15 and 17-21 is improper for at least these reasons. Applicant also respectfully submits that claim 18 would not have been obvious in view of the prior art as relied upon by the Examiner for at least somewhat similar reasons as set forth above with respect to claim 4.

Conclusion

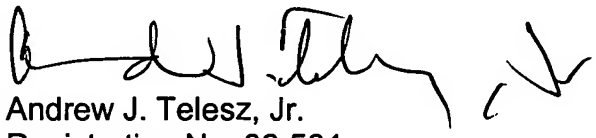
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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